

APR 27 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/655,699
Filing Date September 5, 2003
Inventorship Garo J. Derderian et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Unknown
Attorney's Docket No. MI22-2307
Title: Methods of Depositing a Silicon Dioxide Comprising Layer in the
Fabrication of Integrated Circuitry, Methods of Forming Trench Isolation in
the Fabrication of Integrated Circuitry

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2. Transmittal Form (PTO/SB/21)
3. Cited References (5)

Dated:

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NUMBER OF PAGES IN FACSIMILE: 27

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PTO/SB/21 (03-03)

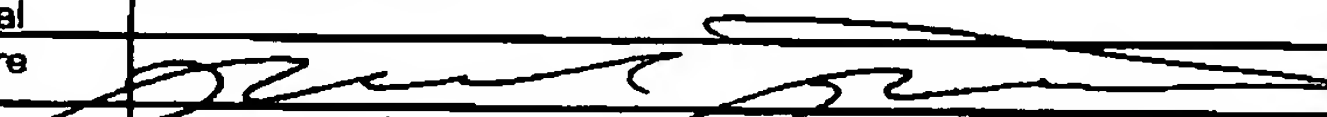
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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	10/655,699
	Filing Date	December 5, 2003
	First Named Inventor	Derderian et al.
	Art Unit	2812
	Examiner Name	Unknown
Total Number of Pages In This Submission	Attorney Docket Number	MI22-2307

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual	Mark S. Matkin, Reg. No. 32,268 Wells St. John, P.S.
Signature	
Date	4-27-05

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. Copies of the cited art are attached hereto. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing of a first Office Action on the merits, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: 4-27-05By: Mark S. Matkin
Reg. No. 32,268

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Sheet 1 of 2

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)	ATTORNEY DOCKET NO. MI22-2307	SERIAL NO. 10/655,699
	APPLICANT: Derderian et al.	
	FILING DATE 12/05/2003	GROUP ART UNIT 2812

U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,013,583	1/11/2000	Ajmera et al.			
	AB	2001/0041250 A1	11/2001	Haukka et al.			
	AC	2002/0000195 A1	1/2002	Kao et al.			
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	AG	2004/0209484	10/2004	Hill et al.			
	AH	2004/0266153 A1	12/30/2004	Yongjun Jeff Hu			

FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AI	EP 0817251 A	1/1998	EPO				
	AJ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
	AK		PCT/US2004/021156; Filed 6/30/2004; Search Report.
EXAMINER	DATE CONSIDERED		
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	APPLICANT: Derderian et al.	
	FILING DATE March 7, 2005	GROUP Unknown

U.S. PATENT DOCUMENTS							
Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AC						
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FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AF							
	AG							
	AH							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)			
	AI		Chen et al., <i>Excimer Laser-Induced Ti Silicidation to Eliminate the Fine-Line Effect for Integrated Circuitry</i>
			<i>Device Fabrication</i> , 149 JOURNAL OF ELECTROCHEMICAL SOCIETY, No. 11, pp. G609-G612 (2002).
	AJ		Nishiyama et al., <i>Agglomeration Resistant Self-Aligned Silicide Process Using N₂ Implantation into TiSi₂</i>
			36 JPN. J. APPL. PHYS., Part 1, No. 6A, pp. 3639-3643 (June 1997).
	AK		Wolf, <i>Chapter 13: Polycides and Salicides of TiSix, CoSi₂, and NiSi</i> , SILICON PROCESSING FOR THE VLSI ERA,
			Vol. IV, pp. 603-604 (pre-2003).
EXAMINER		DATE CONSIDERED	
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